Faculty of Engineering & Technology
P.K.University
Shivpuri (MP)

Evaluation Scheme & Syllabus for
Department Of Electronic Communication engineering

M. Tech -(VLSI Design)
(I to IV Semester)

(Effective from session 2019-20)

EVALUATION SCHEME

M.Tech- VLSI Design

Semester-I

SUBJECT CODE	SUBJECT NAME	THEORY		PRACTICAL		TOTAL
		SESS.(30)	EXT.(70)	SESS.(25)	EXT.(25)	
MTVL-101	Low Power VLSI Design	30	70	NA	NA	100
MTVL-102	FPGA Architecture & Applications	30	70	25	25	150
MTVL-103	Analog VLSI Design	30	70	NA	NA	100
MTVL-104	Testing of VLSI Circuits	30	70	NA	NA	100
MTVL-105	Research Process & Methodology	30	70	NA	NA	100
MTVL-106	VLSI Circuit Design Lab	NA	NA	25	25	50

Semester-II

SUBJECT CODE	SUBJECT NAME	THEORY		PRACTICAL		TOTAL
		SESS.(30)	EXT.(70)	SESS.(25)	EXT.(25)	
MTVL-201	Hardware Description Languages	30	70	NA	NA	100
MTVL-202	VLSI DSP Architectures	30	70	NA	NA	100
MTVL-203	Algorithms for VLSI Design	30	70	NA	NA	100
MTVL-204	VLSI Testing &Testability	30	70	NA	NA	100
MTVL-205	Embedded System for Wireless Comm.	30	70	NA	NA	100
MTVL-206	Advanced VLSI Design Lab	NA	NA	25	25	50
MTVL-207	Seminar-I	NA	NA	25	25	50

Semester-III

SUBJECT CODE	SUBJECT NAME	THEORY		PRACTICAL		TOTAL
		SESS.(30)	EXT.(70)	SESS.(25)	EXT.(25)	
MTVL-301	Dissertation phase-I	NA	NA	200	200	400
MTVL-302	Seminar-II	NA	NA	25	25	50

Semester-IV

SUBJECT CODE	SUBJECT NAME	THEORY		PRACTICAL		TOTAL
		SESS.(30)	EXT.(70)	SESS.(25)	EXT.(25)	
MTVL-401	Dissertation phase-II	NA	NA	300	300	600

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I Year I Semester

MTVL101 –Low Power VLSI Design

UNIT I:

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II:

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III:

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV:

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V:

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI:

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII:

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII:

SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Text Books:

1. Yeo Rofail/ Gohl, CMOS/BiCMOS ULSI low voltage, low power, PearsonEducation.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP.
3. Douglas A.Pucknell& Kamran Eshraghian, Basic VLSI Design, PHI Publication.
4. J.Rabaey, Digital Integrated circuits, PHI Publication.
5. Sung-mo Kang and Yusuf Leblebici, CMOS Digital ICs, TMH Publication .

MTVL102 –FPGA Architecture & Applications

UNIT-I

Programmable Logic ROM, PLA, PAL, PLD, PGA–Features, programming and applications using complex programmable logic devices Altera series–Max 5000/7000 series and Altera FLEX logic–10000 series CPLD, AMD's–CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice PLST's Architectures–3000 Series–Speed Performance and in system programmability.

UNIT-II

FPGAs Field Programmable Gate Arrays–Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs.

UNIT-III

Case Studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T–ORCA's (Optimized Reconfigurable Cell Array): ACTEL's–ACT-1,2,3 and their speed performance.

UNIT-IV

Finite State Machines (FSM)-I Top-down Design–State Transition Table, state assignments for FPGAs,Problem of initial state assignmentfor one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL.

UNIT-V

Finite State Machines (FSM)-IIAlternative realization for state machine chart using microprogramming.Linked state machines,One–Hot statemachine, Petrinetes for statemachines–basic concepts, properties, Extended petrinetes for parallelcontrollers. Finite State Machine–Case Study, Meta Stability,Synchronization.

UNIT-VI

FSM Architectures and Systems Level Design Architectures centered around non-registered PLDs,State machine designs centered around shift registers,One –Hot design method,Use of ASMs in One –Hot design. K Application of One –Hot method, System level design controller, data path and functional partition.

UNIT-VII

Digital front end Digital Design Tools for (FPGAs & ASICs) using Cadence EDA Tool ("FPGA Advantage") –Design Flow Using FPGAs.

UNIT-VIII

Guidelines and Case Studies Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Reference Books:

1. P.K.Chan& S. Mourad, Digital Design using Field ProgrammableGate Array, Prentice Hall.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology,Kluwer Academic Pub.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
4. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray,Kluwer Pub.

MTVL102 –FPGA Design Lab

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ ModelSim tools) using VHDL/Verilog Hardware Description Languages

1. Part – I Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

2. Part – II Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

3. Part – III Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

4. Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD etc

MTVL103 –Analog VLSI Design

Introduction to Analog VLSI

Analog integrated circuit design, Circuit design consideration for MOS challenges in analog circuit design, recent trends in analog VLSI circuits.

Analog MOSFET Modeling

MOS transistor, Low frequency MOSFET Models, High frequency MOSFET Models,

temperature effects in MOSFET, Noise in MOSFET.

Current Source, Sinks and References

MOS Diode/Active resistor, Simple current sinks and mirror, Basic current mirrors, advance current mirror, Current and Voltage references, band gap references.

CMOS Amplifier

Performances matrices of amplifier circuits, Common source amplifier, Common gate amplifier, Cascode amplifier, Frequency response of amplifiers and stability of amplifier.

CMOS Feedback Amplifier

Feedback equation, Properties of negative feedback on amplifier design, Feedback Topology, Stability.

CMOS Differential Amplifier

Differential signalling, source coupled pair, Current source load, Common mode rejection ratio, CMOS Differential amplifier with current mirror load,, Differential to single ended conversion.

CMOS Operational amplifier

Block diagram of Op-amplifier, Ideal characteristics of Op-Amplifier, Design of two stage Op-Amplifier, Compensation of Op-Amplifier, Frequency response of Op-Amplifier, Operational Trans conductance Amplifier (OTA).

CMOS Comparator

Characteristic of a comparator, Two stage open loop comparator, Special purpose comparator, Regenerative comparator, High output current amplifier, High speed comparator.

Switched Capacitor Circuits

Switched capacitor circuits, Switched capacitor amplifiers, Switch capacitor integrators.

Text Book:

1. BehzadRazavi , “Design of Analog CMOS Integrated Circuits”, McGraw Hill Publication.
2. R. Jacob Baker, Harry W. Li, and David E. Boyce,“CMOS: Circuit Design , Layout and Simulation”, Prentice Hall of India
3. David A. Johns and Ken Martin, “Analog Integrated circuit Design, John Wiley & Sons.

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I Year I Semester

MTVL104 – Testing of VLSI Circuits

UNIT I

BASICS OF TESTING AND FAULT MODELING Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling - Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation

UNIT II

TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS Test generation basics - test generation algorithms - path sensitization - Boolean difference – Dalgorithm – PODEM - Testable combinational logic circuit design.

UNIT III

TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan

UNIT IV

MEMORY, DELAY FAULT AND IDDQ TESTING Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing - testing methods - limitations of IDDQ Testing

UNIT V

BUILT-IN SELF-TEST Test pattern generation of Built-in Self-Test (BIST) - Output response analysis – BIST architectures.

Reference Books:

1. P. K. Lala, "Digital Circuit Testing and Testability", Academic Press.
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers.
3. N.K. Jha and S.G. Gupta, "Testing of Digital Systems", Cambridge University Press.
4. ZainalabeNavabi, "Digital System Test and Testable Design: Using HDL Models and Architectures", Springer.

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I Year I Semester

MTVL105: Research Process and Methodology

UNIT 1:

Introduction to Research and Problem Definition-Meaning, Objective and importance of research, Types of research, steps involved in research, defining research problem

UNIT 2:

Research Design-Research design, Methods of research design, research process and steps involved, Literature Survey

UNIT 3:

Data Collection-Classification of Data, Methods of Data Collection, Sampling, Sampling techniques procedure and methods, Ethical considerations in research

UNIT 4:

Data Analysis and interpretation-Data analysis, Statistical techniques and choosing an appropriate statistical technique, Hypothesis, Hypothesis testing, Data processing software (e.g. SPSS etc.), statistical inference, Interpretation of results

UNIT 5:

Technical Writing and reporting of research-Types of research report: Dissertation and Thesis, research paper, review article, short communication, conference presentation etc., Referencing and referencing styles, Research Journals, Indexing and citation of Journals, Intellectual property, Plagiarism

Text Books:

1. C. R. Kothari, Gaurav Garg, Research Methodology Methods and Techniques , New Age International publishers, Third Edition.
2. Ranjit Kumar, Research Methodology: A Step-by-Step Guide for Beginners, 2nd Edition, SAGE, 2005
3. Business Research Methods – Donald Cooper & Pamela Schindler, TMGH, 9th edition
4. Creswell, John W. Research design: Qualitative, quantitative, and mixed methods approaches. Sage publications, 2013.

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I Year I Semester

MTVL106 – VLSI Circuit Design Lab

Experiments shall be carried out using Tanner/Mentor Graphics/Cadence/Xilinx Tools

Session – I: Digital IC Design Laboratory

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)

2. Modeling of Diodes, MOS transistors, Bipolar Transistors etc using SPICE.

3. An Overview of Tanner EDA Tool/MicroWind/Electric/ Magic/LTSpice

4. I-V Curves of NMOS and PMOS Transistors

5. DC Characteristics of CMOS Inverters (VTC, Noise Margin)

6. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation)

7. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits

8. Schematic Entry/Simulation/ Layout of CMOS Sequential Circuits

9. High Speed and Low Power Design of CMOS Circuits

Session-II: Analog IC Design Laboratory

1. Study of MOS Characteristics and Characterization

2. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier)

3. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier)

4. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing)

5. Design and Simulation of Basic Current Mirror, Cascode Current Mirror

6. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier

7. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier

MTVL201 –Hardware Description Languages

UNIT –I

HARDWARE MODELING WITH THE VERILOG HDL : Hardware Encapsulation –The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis ,Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOGHDL: User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions ,Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non- Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology- Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don t Cares, Synthesis of Sequential Logic Synthesis of Sequential Udps, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures.

UNIT V

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User- Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT VI

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic. Design Examples in Verilog.

UNIT VIII

NTRODUCTION TO VHDL: An Overview of Design Procedures used for System Design using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples using Commercial PC Based on VHDL Elements of VHDL Top Down Design with VHDL Subprograms. Controller Description VHDL Operators.

UNIT VIII

BEHAVIORAL DESCRIPTION OF HARDWARE IN VHDL: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design. Differences between VHDL and Verilog.

Reference Books:

1. M.D.CILETTI, Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Prentice-Hall.
2. Z.NAWABI, VHDL Analysis and Modeling of Digital Systems, McGraw Hill.
3. M.G.ARNOLD, Verilog Digital – Computer Design", Prentice-Hall (PTR).
4. PERRY, "VHDL", McGraw Hill.

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I Year II Semester

MTVL202 –VLSI DSP Architectures

Essential features of Instruction set architectures of CISC, RISC and DSP processors and their implications for Implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance: Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls.

Data path and control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls.

Enhancing performance with pipelining: An overview of pipelining, a pipe lined data path, pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards, using a hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

Computational accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP systems, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D/A conversion errors.

Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

Text Books:

1. D.A, Patterson, J.L. Hennessy, Computer Organization and Design: Hardware / Software Interface, 4th Edition, Elsevier.
2. A.S. Tannenbaum, Structured Computer Organization, 4th Edition, Prentice-Hall
3. W. Wolf, Modern VLSI Design: Systems on Silicon, 2nd Edition, Pearson Education
4. KeshabParhi, VLSI digital signal processing systems design and implementations, Wiley
5. Avatar Sigh, Srinivasan S, Digital signal processing implementations using DSP microprocessors with examples, Thomson.

MTVL203 – Algorithms for VLSI Design

VLSI physical design automation and Fabrication VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI automation Algorithms Partitioning: Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.

Floor planning & pin assignment: Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block& cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement .

Global Routing and Detailed routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

Over the cell routing & via minimization: Two layers over the cell routers, constrained & unconstrained via minimization

Compaction: Problem formulation, classification of compaction algorithms, one-dimensional compaction, two dimension based compaction, hierarchical compaction Reference

Books : 1. Naveed Shervani, "Algorithms for VLSI physical design Automation", KluwerAcademic Publisher, Second edition.

2. ChristophnMeinel& Thorsten Theobold, "Algorithm and Data Structures for VLSIDesign", Kluwer Academic Publisher.
3. R. Drechsler, "Evolutionary Algorithm for VLSI CAD", Kluwer Academic Publication.

MTVL204 –VLSI Testing and Testability

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends Affecting Testing.

VLSI Testing Process and Test Equipment: How to Test Chips? Automatic Test Equipment, Electrical Parametric Testing. Faults in Digital Circuits: Failures and Faults, Modeling of Faults, Temporary Faults.

Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits, Test Generation Techniques for Combinational Circuits, Detection of Multiple Faults in Combinational Logic Circuits. Testable Combinational Logic Circuit Design: The Reed-Mullar Expansion Technique, Three-Level OR-AND-OR Design, Automatic Synthesis of Testing Logic, Testable Design of Multilevel Combinational Circuits, Synthesis of Random Pattern Testable Combinational Circuits, Path Delay Fault Testable Combinational Logic Design, Testable PLA Design.

Test Generation for Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure, Functional Fault Models, Test Generation Based on Functional Fault Models.

Design of Testable Sequential Circuits: Controllability and Observ ability, Ad Hoc Design Rules for Improving Testability, Design of Diagnosable Sequential Circuits, The Scan-Path Technique for Testable Sequential Circuit Design, Level-Sensitive Scan Design, Random

Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Non scan Techniques, Cross Check, Boundary Scan.

Built-In Self-Test: Test Pattern Generation for BIST, Output Response Analysis, Circular BIST, BIST Architectures.

Testable Memory Design: RAM Fault Models, Test Algorithms for RAMs, Detection of Pattern Sensitive Faults, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

Text Books:

1. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.
2. M.L. Bushnell and V.D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.

MTVL205 –Embedded System for Wireless & Mobile Communication

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology.

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatter net Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile,

Secondary bluetooth profile Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

Programming with Java: Java Programming, J2ME architecture, Javax. bluetooth package Interface, classes, exceptions, Javax. obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application.

Overview of IrDA, HomeRF, Wireless LANs, JINI

Reference Books:

1. C.S.R. Prabhu and A.P. Reddi,“ Bluetooth Technology”, PHI Publication.
2. U. Dalal& M. Shukla, "Wireless & Mobile Communication", Oxford University Press.
3. C. Y. William, Lee, "Mobile communication engineering theory and applications", TMH, Publication.
4. S .Haykins, “Communication Systems”, John Wiley and Sons.

MTVL206 – Advanced VLSI Design Lab

Session-I: VLSI System Design

1. Design/Simulation of other analog building blocks
a. Comparators
b. Oscillators
c. PLLs
d. switched capacitor circuits
e. Noise Analysis

2. Mini Projects involving
a. Unpipelined MIPS Processor
b. Pipelined MIPS Processor
c. Out of Order Execution with Tomasulo's Algorithm
d. Communication Controllers
e. Arithmetic Circuits
f. DSP Systems

Session-II: ASIC Design

Experiments shall be carried out using Mentor Graphics/Cadence Tools

1. Part-I: Backend Design

Schematic Entry/ Simulation / Layout/ DRC/PEX/Post Layout Simulation of CMOS Inverter, NAND Gate, OR Gate, Flip Flops, Register Cell, Half Adder, Full Adder Circuits

2. Part-II: Semicustom Design

HDL Design Entry/ Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power Analysis of Medium Scale Combinational, Sequential Circuits

3. Part-III: High Speed/Low Power CMOS Design

Designing combinational/sequential CMOS circuits for High Speed

Designing combinational/sequential CMOS circuits for LowPower.